

RESEARCH ARTICLE

A magnetic-core based fault current limiter for utility applications

S.K. Abeygunawardane¹, J.R.S. Sisira Kumara¹, J.B. Ekanayake^{2*} and A. Arulampalam¹

¹ Department of Electrical and Electronic Engineering, Faculty of Engineering, University of Peradeniya, Peradeniya.

² Cardiff School of Engineering, Cardiff University, Wales, UK.

Revised: 28 August 2010 ; Accepted: 20 May 2011

Abstract: A magnetic core fault current limiter (MFCL) saturated by a dc biasing coil was designed and implemented, both experimentally and in PSCAD/EMTDC simulation package. The operation of the device under normal operating conditions and faults was then studied. A case study was carried out using simulation to demonstrate the application of the proposed MFCL. The benefits of using a grid-connected single-phase rectifier to bias the dc coil of the MFCL were investigated through simulation studies. The simulation results show improvements in limiting the fault current and minimizing the voltage sag on healthy busbars during a fault. It was also found that the highest improvements are achieved when the rectifier is connected to the downstream grid.

Keywords: Distributed generators, distribution network, magnetic fault current limiter.

INTRODUCTION

Many countries around the world are setting targets to decarbonise the electrical power sector. One of the possible options for supporting the decarbonisation is connecting small renewable energy sources to the distribution network. These generators are commonly known as distributed generators (DG). In Sri Lanka as at August 2010, 211 MW (170 MW micro-hydro, 11 MW biomass and 30 MW wind) of DGs were already connected to the distribution network and another 137 MW (70 MW micro-hydro, 2 MW biomass and 65 MW wind) of DGs were in the pipeline for connection. These generators are normally connected in remote areas where distribution network resources are operating near their limits. The switchgear is one of the power system equipments, which constraint the connection of DGs. The fault current contribution of DGs causes higher fault current levels thus exceeding the short circuit ratings of switchgear. Upgrading the switchgear is not economical and may incur longer interruptions. Therefore, the

introduction of fault current limiting devices (Mumford, 1995; Power, 1995; Kovalsky *et al.*, 2005) has been considered by many utilities.

The fault current limiter (FCL) is connected in series with the power line and shows zero or low impedance during normal loading conditions and high impedance during faults. According to the technologies used to obtain the required impedance characteristic, FCL can be categorized into three main groups: (a) superconducting fault current limiter (SFCL) (Mumford, 1995; Power, 1995; Yu *et al.*, 2001), (b) magnetic fault current limiter (MFCL) (Iwahara *et al.*, 1999; Yu *et al.*, 2001) and (c) static fault current limiter (StFCL) (Putrus *et al.*, 1995; Salim *et al.*, 2004). In addition to these three, there are FCL devices, which can be identified as a combination of the above types. The different types of FCL devices have their own advantages and disadvantages. In terms of performance, SFCL is superior to the other two; whereas in terms of the cost and ease of implementation, MFCL and StFCL are preferred choices (SFCL required a liquid nitrogen bath referred to as 'cryostat').

The MFCL can broadly be divided into three categories, namely, modified B-H characteristic type, superconducting coil type and dc biasing type. In the modified B-H characteristic type FCLs a piece-wise B-H characteristic is obtained by embedding permanent magnets into a selected steel core (Mukhopadhyay *et al.*, 1998, 1999). The combination of the permanent magnets and the steel core is selected to shape the B-H curve such that it has a piece-wise linear characteristic showing a low impedance to normal load currents and higher impedance to fault currents. A slightly different approach using only one permanent magnet was presented by Iwidiara *et al.* (1999). Calman *et al.* (2001) discussed a passive magnetic fault current limiter based on permanent magnets. An

* Corresponding author (ekanayakej@cardiff.ac.uk)

MFCL employing a permanent magnet having a large square hysteresis was presented in a previous study (Rasolonjanahary *et al.*, 2005). During the first peak of a fault, the large fault current cycles around this large hysteresis loop, thus dissipating large amount of energy, which would otherwise pass into the fault. This in turn limits the fault current.

The fault current limiters based on a high temperature superconducting biasing coil, which can drive the magnetic core into saturation by a dc current can be found in previous studies (Kcilin *et al.*, 2000; Hoshino *et al.*, 2003).

The dc biasing type uses a similar principle as the superconductor coil type approach, where a dc bias is used to drive the core into saturation. Salim *et al.* (2002) presents the operating principles and experimental results of an FCL where the dc bias coil is fed from an isolated dc source. Another approach where the dc bias coil is located on a closed elongated magnetic core and disconnected during a fault using a control circuit triggered by the voltage drop across the FCL terminals has been discussed earlier (Rozenstein *et al.*, 2007).

The work presented in this paper extends the basic idea presented in a previous study (Salim *et al.*, 2002) and discusses the application of a single-phase rectifier as the dc biasing sources for MFCLs in each phase. The advantages that can be gained in terms of limiting current and minimizing the voltage sag on the healthy busbars are shown by connecting the rectifier to the upstream and downstream busbars of the FCL.

METHODS AND MATERIALS

Saturated core magnetic fault current limiter:

a) principle of operation: A saturated core MFCL (Figure 1) consists of two magnetic cores, each having two coils wound on the core. One coil is connected to the power line in series and the other coil is connected to a dc source. The two cores are biased in opposite directions where one core offers current limiting for one half cycle of the ac waveform while the other core is responsible for the other half cycle.

The principle of operation of the MFCL is described by considering one magnetic core. As shown in Figure 2, the dc current supply to the dc coil produces a magnetic field, which increases the flux density of the core in such a way to drive the core into saturation. The normal load current produces a varying magnetic field, which superimposes on the dc operating point. As illustrated in

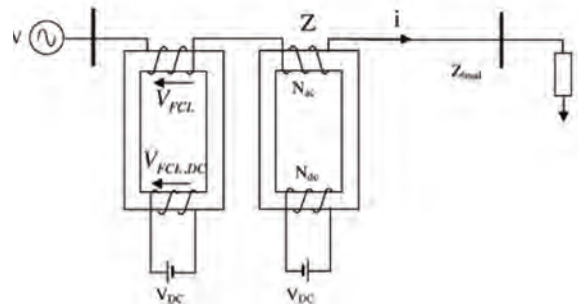


Figure 1: Full cycle saturated core MFCL

V_{FCL} - voltage induced across the ac coil, $V_{FCL,DC}$ - voltage induced across the dc coil, N_{ac} - number of turns in the ac coil, N_{dc} - number of turns in the dc coil, V - voltage at the generator busbar, V_{DC} - biasing voltage, Z - line impedance, Z_{load} - load impedance

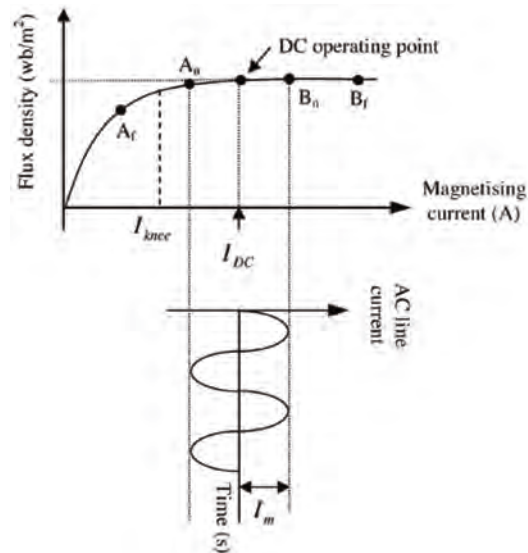


Figure 2: Flux change of the MFCL in normal operation

I_{DC} - biasing current, I_m - peak value of ac line current, I_{knee} - magnetizing current at the knee point

Figure 2, this relatively low ac magnetic field swings the operating point between A_n and B_n . During the negative half cycle of the ac waveform (where operating point moves to A_n), the flux density is changing slightly thus introducing a small impedance in series with the ac line.

During a fault due to a large current flow in the core, the operating point swings from A_f to B_f . The ac magnetic field produced by the fault current brings the core out of saturation (point A_f) during the negative half cycle of the current. As core comes to the linear region

of the magnetising curve, the device shows a large series impedance (this is the absolute impedance seen by the current) to ac current. Similarly the core, which is saturated in the reverse direction (see the second core in Figure 1) shows a large series impedance during the positive half cycle of the ac waveform. Therefore the device with two magnetic cores acts as a limiting impedance for the current flowing in the power line.

b) design considerations: The design of a core is based on both the required performance during current limiting and normal loading. Obtaining the most effective design in terms of performance and cost is determined by a number of design parameters, namely, the core material, dimensions of the core, number of turns in the primary and secondary windings, and the magnitude of the dc voltage that is required to bias the core. In this section, important design considerations involved in the design of a saturated core MFCL are briefly described (Metha, 2001; Hughes, 2004).

When the core comes out of saturation, a voltage, V_{FCL} , will be induced across the FCL and it can be expressed as:

$$V_{FCL} = N_{ac} \frac{d\phi}{dt} \quad \dots(1)$$

Since the flux (ϕ) is varying sinusoidally, $\phi = \phi_m \sin \omega t$, equation (1) was modified to:

$$V_{FCL} = N_{ac} \phi_m \omega \cos \omega t$$

$$V_{FCL,max} = N_{ac} \phi_m \omega = 2\pi N_{ac} B_m A_f \quad \dots(2)$$

The maximum value of the induced voltage, $V_{FCL,max}$, was calculated by the impedance at point A_r (Figure 2) and the fault current.

During the normal operation at the negative peak of the ac current, the operating point of the core moves to point A_n (Figure 2). In order to keep the core in saturation region during the negative half of the ac current, the dc bias current should satisfy (3):

$$I_{DC} - I_m > I_{knee} \quad \dots(3)$$

When the core comes out of saturation it acts as a transformer and a voltage is induced across the dc winding ($V_{FCL,DC}$) as shown in Figure 1. The dc source should be able to drive enough current to satisfy equation (3) even with the presence of $V_{FCL,DC}$. That is given by

$$\frac{V_{DC} - V_{FCL,DC}}{R_{DC}} > I_{knee} \quad \dots(4)$$

In equation (4), R_{DC} is the resistance of the dc winding. It is expressed in terms of the resistivity of the coil wire ρ , the average length of a single turn l_t , the number of turns of the dc winding, N_{dc} and the cross sectional area of the coil, A_{dc} as:

$$R_{DC} = \frac{\rho N_{dc} l_t}{A_{dc}} \quad \dots(5)$$

Magnetising current (I) in the core is related to the magnetic field intensity H , as:

$$H = \frac{N \times I}{l} \quad \dots(6)$$

where l is the mean length of the core and N is the number of turns in the winding.

Equations (2), (4), (5) and (6) together with the B-H curve of the core material were used to design the number of turns in the ac and dc windings, and the voltage of the dc source.

c) prototype design and implementation: For the laboratory prototype, the test system shown in Figure 3 was used. The load resistance (R_{load}) in this test system was selected as 50Ω , which gives a load current of 1 A. As for distribution networks the fault current is 5 – 20 times the load current (IEEE 242-2001) and in this laboratory setup the fault current was set to 10 A. In order to obtain a fault current of 10 A, R_{fault} was selected as 5Ω . The MFCL was designed to limit the fault current to 5 A. R_{fault} was adjusted to obtain the required voltage and current from the dc voltage source.

Assuming that the core is made out of grain oriented core steel, the design procedure outlined in the previous section was used to design the laboratory scale MFCL. The design parameters selected for the MFCL is given in Table 1. The design was based on an available core and the data for the core is given in Annex A. As the number of equations available for the design is less than the design parameters, the design was carried out by fixing the number of turns on the dc winding to 40.

The prototype was implemented both experimentally and using the simulation package PSCAD/EMTDC. The experimental rig was based on a single core, which is acting on the positive half cycle whereas both cores as shown in Figure 1 was used for simulations. Test results are provided under “results and discussion” section.

Case study:

a) network configuration: The distribution network shown in Figure 4 was selected for the case study. The

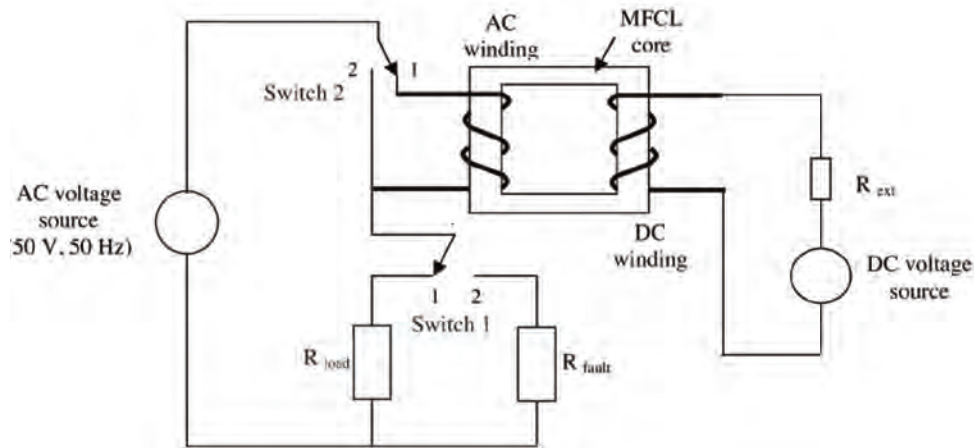


Figure 3: Laboratory test system

11 kV distribution network is supplied by a 10 MVA, 33/11 kV transformer, which is connected to the 33 kV, 750 MVA grid supply point (GSP) by a 30 km long aluminum conductor, steel reinforced (ACSR) 75 mm² overhead transmission line. In addition to that a 11 kV, 4.51 MVA DG is connected to a 11 kV busbar. A 16 km ACSR, 100 mm² overhead line is connected to 11 kV busbar as a primary distribution feeder. This line supplies 5 loads, which are rated at 0.6 MW and 0.3 Mvar, through 1.6 MVA, 11 kV/0.415 kV distribution transformers. The five loads: Load 1, Load 2, Load 3, Load 4 and Load 5 are located at 0 km, 4 km, 8 km, 12 km and 16 km away from the starting point.

The MFCL was located at the starting point of the distribution feeder (Figure 4). The MFCL described in the previous section was modified by introducing a single-phase rectifier (Figure 5), which is used to bias the

magnetic core towards saturation. The effect of obtaining the ac supply for the rectifier from busbar A or B was investigated. During a fault in downstream, the voltage drop across the MFCL was relatively high. The voltage at busbar A was constant and kept closer to the system voltage; whereas the voltage at busbar B dropped during a fault.

As shown in Annex B, one phase of the distribution network was modelled in PSCAD/EMTDC software package. Two single phase saturable transformers with 1:1 turn ratio and rated voltage of 4 kV was selected for the MFCL cores. A single phase rectifier, which is connected to the mains network by means of a 6.35 kV/1.41 kV transformer, was used to feed the biasing coil of the saturable transformer. The dc side of the rectifier was connected to the dc winding of the MFCL with a series resistor of 2.5 Ω .

Table 1: Selected parameters to design the MFCL

Parameter	Unit	Value
Width of core laminations (w)	cm	8
Length of a side of the core (x and y)	cm	36.6
Thickness of the core (t)	cm	3.7
No. of turns in ac winding	Nos	18
Gauge of the coil in ac winding		21
No. of turns in dc winding	Nos	40
Gauge of the coil in dc winding		19
Bias current, I_{dc}	A	2
Voltage to the dc winding, V_{dc}	V	3.6

Table 2: Event summary of simulation

Time period		Event
Start time of the event	End time of the event	
0	1	Normal loading
1	2	Line to Ground Fault at Load 5
2	3	Line to Ground Fault at Load 4
3	4	Line to Ground Fault at Load 3
4	5	Line to Ground Fault at Load 2
5	6	Line to Ground Fault at Load 1
6	7	Line to Ground Fault at Busbar B
7	8	Normal loading

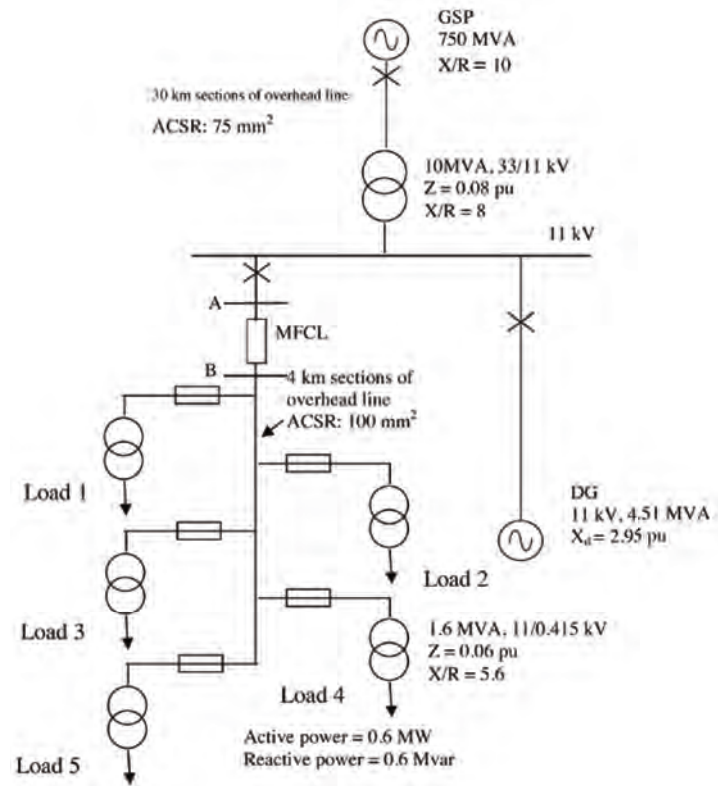


Figure 4: Single line diagram of the network

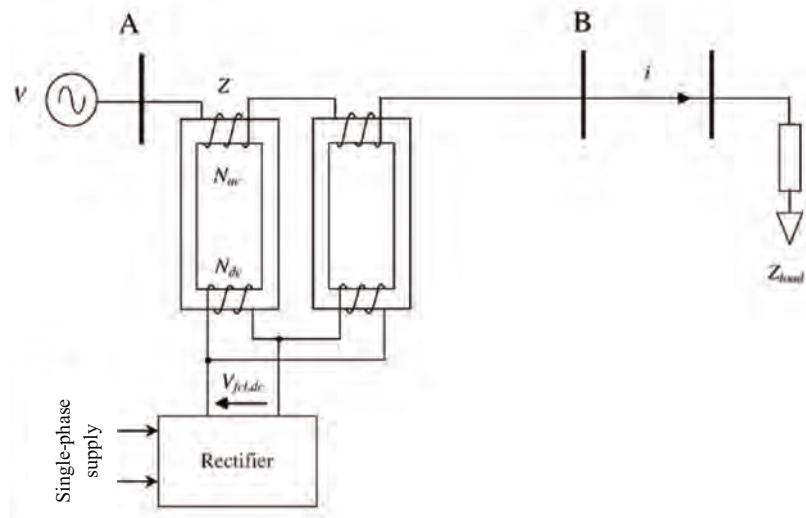


Figure 5: Connection of saturated core MFCL- rectifier at generator busbar

N_{ac} - number of turns in the ac coil, N_{dc} - number of turns in the dc coil, $V_{fcl,dc}$ - voltage induced across the dc coil, Z - line impedance, Z_{load} - load impedance

b) simulation: Using the developed model simulation studies were carried out without DG [case (a)] and with DG for four different cases (b), (c), (d) and (e) :

- the operation of the network without the DG and MFCL,
- the operation of the network without the MFCL,
- the operation with the MFCL, which was biased from a constant dc source,
- the operation with the MFCL, which was biased from a rectifier connected to busbar A (upstream busbar), and
- the operation with the MFCL, which was biased from a rectifier connected to busbar B (downstream busbar).

For each case simulation was run for 8 sec and a series of events, given in Table 2, was applied to the network.

RESULTS AND DISCUSSION

Performance of the laboratory prototype

The laboratory prototype was tested under: normal loading without MFCL, normal loading with MFCL, a fault without MFCL, and a fault with MFCL. The current waveforms for each case was obtained and are shown in

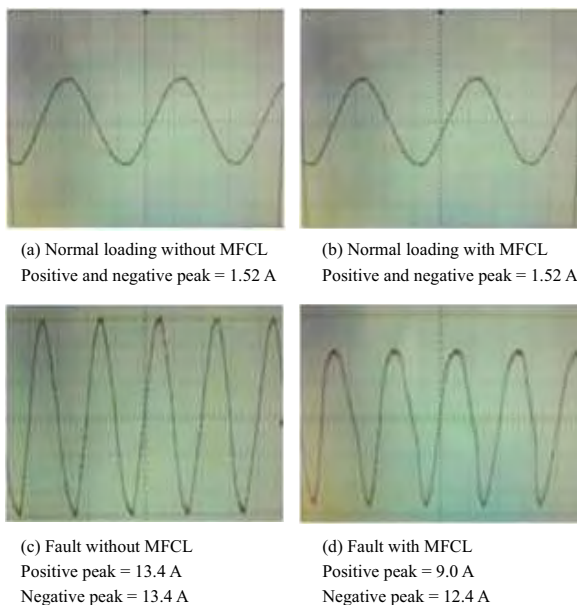


Figure 6: Current waveforms with and without the FCL

Figure 6. The peak values of the currents are also given in the relevant oscillograms. From the results it can be observed that application of the MFCL has not changed the current under normal loading condition, but it limits the current during a fault. Even though it was designed to limit the current by 50% during the positive half cycle, it limited the current by 32.8% during the positive half cycle and by 7.5% during the negative half cycle. This is due to the resistive fault impedance in the prototype, which created a phase shift between supply voltage and voltage drop across the FCL. Also the voltage drop across the FCL is not sinusoidal as the core is not having a perfect linear region.

Simulation results with both cores

In order to investigate the expected operation of the MFCL with both cores, the prototype was tested using the simulations. The MFCL was connected at 0.5 s. Figure 7 shows the current without (from 0 – 0.5 s) and with (0.5 s onwards) the MFCL.

As can be seen from the bottom traces of Figures 6 and 7, the peak value of the fault current with and without the MFCL is approximately equal.

Case study

Figure 8 shows the variation of the line current (rms value of the current flowing through busbar B) with the time for all five events defined in Table 2. During normal loading condition the current was about 160 A and same for all four cases. As can be seen from the plots for cases (a) and (b), the fault current increases when the DG is connected to the network. From plots (c) to (e), it can be clearly seen that the MFCL limited the fault current with different limiting capabilities. The MFCL with rectifier connected to the load busbar [case(e)] was offering the maximum limiting capability irrespective of the fault location. This is mainly due to the drop in voltage at

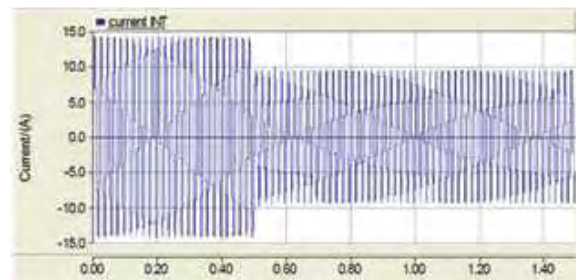


Figure 7: Simulation results

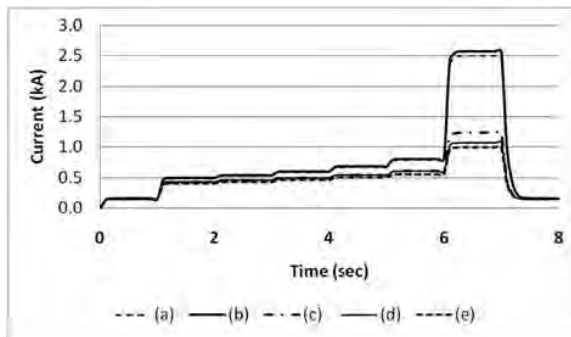


Figure 8: Variation of line current flow through busbar B

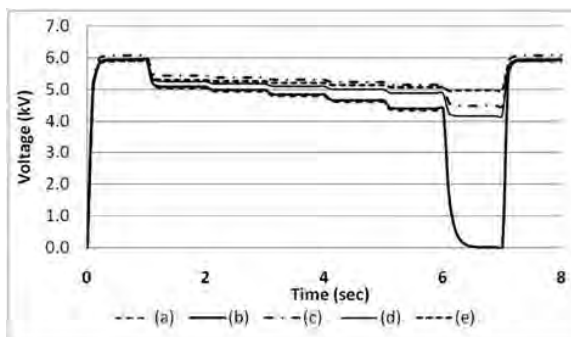


Figure 9: Variation of voltage at generator busbar (busbar A)

busbar B during a fault. The single-phase supply to the rectifier drops thus reducing the dc biasing current. This in turn shifts the dc operating point shown in Figure 2 towards the unsaturated region. Therefore the current limiting was aided by two actions namely, the shift of the dc operating point towards the unsaturated region and the attenuation caused by the large ac fault current as shown in Figure 2.

The variation of phase voltage at 11 kV generator busbar (busbar A) for all four cases was recorded and shown in Figure 9. As can be seen from the plots for cases (a) and (b), without the MFCL the remote faults only create a voltage sag of about 30% on busbar A. A fault at busbar B brings the voltage at busbar A almost down to zero. The application of the MFCL maintains the voltage at busbar A above 80% of the nominal for all the faults. This is an important observation, which clearly indicates that a fault on the network connected to busbar B has little effect on the other loads or networks connected to busbar A when the MFCL is present in between busbars A and B. It is worth mentioning that the voltage at busbar B is governed by the location of the fault and the impedance to the fault.

CONCLUSION

A design and operation of a saturated core MFCL was investigated both using simulations and a laboratory scale prototype. The application of a single-phase rectifier to bias the MFCL was studied. The use of separate single-phase rectifiers for three phases provides added advantages due to the decoupled operation of three MFCLs. This is important during single phase faults as only the dc bias of the MFCL in the faulty phase is changing, without affecting the healthy phases. However, further investigations are required to study the effect of the single-phase rectifier based MFCLs on the fault current during asymmetrical fault conditions.

From simulations it was also shown that the current limiting ensures voltage at busbar A above 80%. This in turn facilitates the DG to ride through a fault without aid of any other auxiliary control or devices. The MFCL also improves the voltage seen by the loads connected to the upstream grid, during a fault.

Even though this more practical approach provides performance improvement, further studies are required to investigate the effect of different parameters such as the core material and the number of turns in each coil on the cost and size of the MFCL.

REFERENCES

1. Calman S., Dawson F.P., Yamada S. & Iwahara M. (2001). Design improvements to a three-material passive magnetic current limiter. *IEEE Transactions on Magnetics* **37**(04): 2624 – 2626.
2. Hoshino T., Salim K.M., Kawasaki A. & Muta I. (2003). Design of 6.6 kV, 100 A saturated DC reactor type superconducting fault current limiter. *IEEE Transactions on Applied Superconductivity* **13**(02): 2012-2015.
3. Hughes E. (2004). *Hughes Electrical Technology*, 8th edition, 3rd reprint, pp. 127-153. Pearson Education, New Jersey, USA.
4. IEEE 242-2001 (2001). *IEEE Recommended Practice for the Protection and Coordination of Industrial and Commercial Power Systems* (IEEE Buff Book). IEEE Standards Association, New Jersey, USA.
5. Iwahara M., Mukhopadhyay S.C., Yamada S. & Dawson F. P. (1999). Development of passive fault current limiter in parallel biasing mode. *IEEE Transactions on Magnetics* **35**(05): 3523-3525.
6. Kcilin V., Kovalcev I., Kmglov S., Stepanov V., Slmgav I. & Shchrbzkov V. (2000). Model of HTS three-phase saturated core fault current limiter. *IEEE Transactions on Applied Superconductivity* **10**(01): 836 – 839.
7. Kovalsky L., Xian Y., Tekletsadik K., Keri A., Bock J. & Breuer F. (2005). Application of superconducting fault current limiters in electric power transmission systems.

- IEEE Transactions on Applied Superconductivity* **15**(02): 2130-2133.
8. Metha V.K. (2001). *Principles of Electrical Engineering and Electronics*. 1st edition, pp. 139-207. S. Chand & Company LTD., New Delhi, India.
 9. Mukhopadhyay S.C., Iwahara M. & Yamada S. (1998). Investigation of the performances of a permanent magnet biased fault current limiting reactor with a steel core. *IEEE Transactions on Magnetics* **34**(04): 2150-2152.
 10. Mukhopadhyay S.C., Dawson F.P., Iwahara M. & Yamada S. (1999). Analysis, design and experimental results for a passive current limiting device. *IEE Proceedings - Electric Power Applications* **146**(03): 309-316.
 11. Mumford F. (1995). Superconducting fault current limiters *IEE Colloquium on Fault Current Limiters - A Look at Tomorrow*. 08 June 1995: 6/1-6/7.
 12. Power A. J. (1995). An overview of transmission fault current limiters *IEE Colloquium on Fault Current Limiters - A Look at Tomorrow*. 08 June 1995: 1/1-1/5.
 13. Putrus G.A., Jenkins N. & Cooper C.B. (1995). A static fault current limiting and interrupting device. *IEE Colloquium on Fault Current Limiters - A Look at Tomorrow*. 08 June 1995: 5/1-5/6.
 14. Rasolonjanahary J. L., Sturgess J. & Chong E. (2005). Design and construction of a magnetic fault current limiter. *UK Magnetics Society Meeting*, Stamford, UK.
 15. Rozenshtein V., Friedman A., Wolfus Y., Kopansky F., Perel E., Yeshurun Y., Bar-Haim Z., Ron Z., Harel E. & Pundak N. (2007). Saturated cores FCL-a new approach. *IEEE Transactions on Applied Superconductivity* **17**(02): 1756-1759.
 16. Salim K.M., Hoshino T., Nishikawa M., Muta I. & Nakamura T. (2002). Preliminary experiments on saturated DC reactor type fault current limiter. *IEEE Transactions on Applied Superconductivity* **12**(01): 872-875.
 17. Salim K.M., Muta I., Hoshino T., Nakamura T. & Yamada M. (2004). Proposal of DC shield reactor type superconducting fault current limiter. *Cryogenics* **44**(03): 171-176.
 18. Ying X., Weizhi G., Xiaoye N., Zhengjian C., Jingyin Z., Bo T., Haixia X., Yang W., Hui H., Yong Z., Bo H. & Xicheng Y. (2007). Development of saturated iron core HTS fault current limiters. *IEEE Transactions on Applied Superconductivity* **17**(02): 1760-1763.
 19. Yu J., Shi D., Duan X., Tang Y. & Cheng S. (2001). Comparison of superconducting fault current limiter in power system. *IEEE Power Engineering Society Summer Meeting* **1**: 43-47.

Annex A

Material used to make the core was grain oriented core steel and the following designed values were obtained from the B-H curve.

At the knee point:

$$B_{\text{knee}} = 1.7\text{T}$$

$$H = 48\text{ H}$$

On saturation:

$$B_{\text{max}} = 2.1\text{T}$$

$$B = 1.75\text{ T}$$

$$H = 70\text{ H}$$

Annex B

The PSCAD/EMTDC implementation of the proposed network:

